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Grace Semiconductor Manufacturing Corporation

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上海宏力半导体制造有限公司
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Chinese Automotive Electronic Market & MCU Technology Platform Solution

中国汽车电子市场及MCU工艺解决方案

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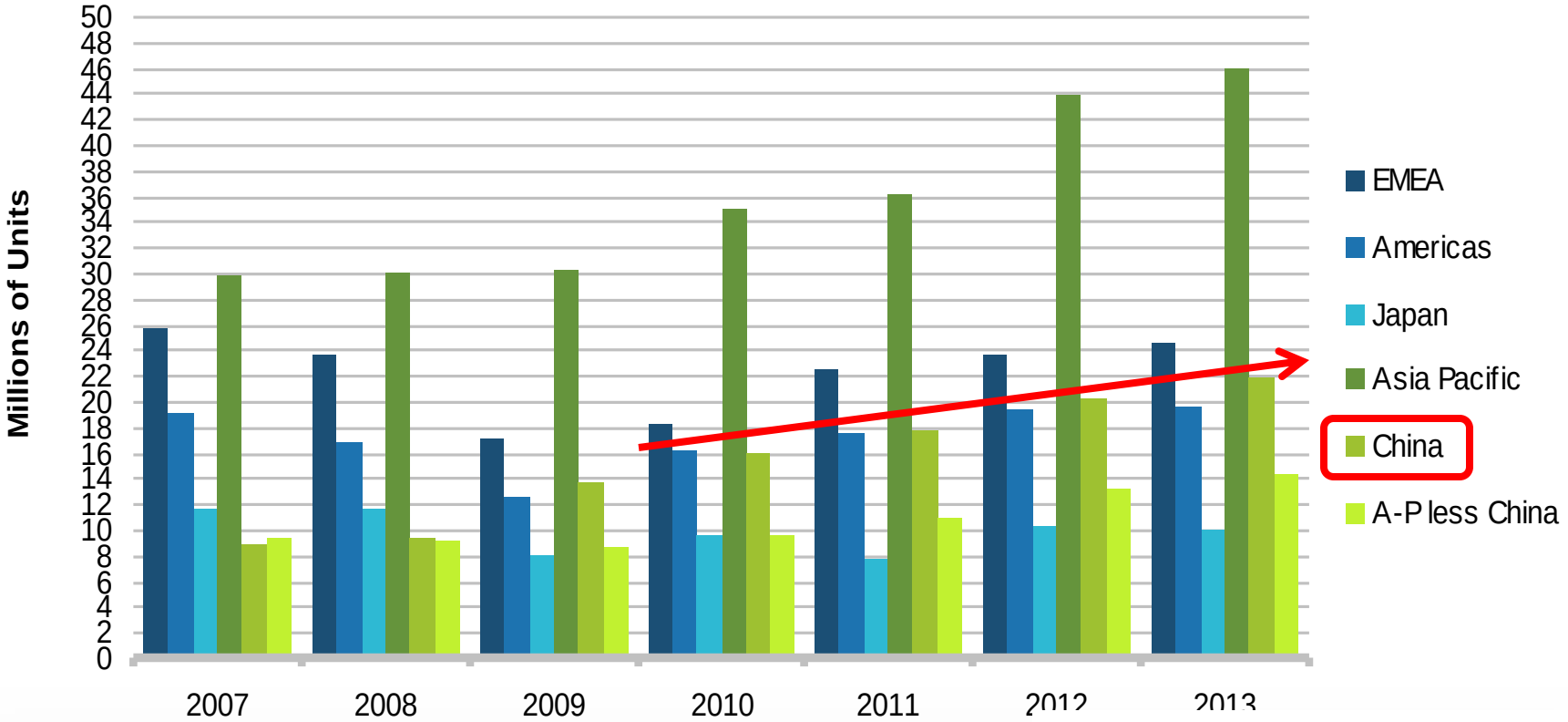
Content

Outline

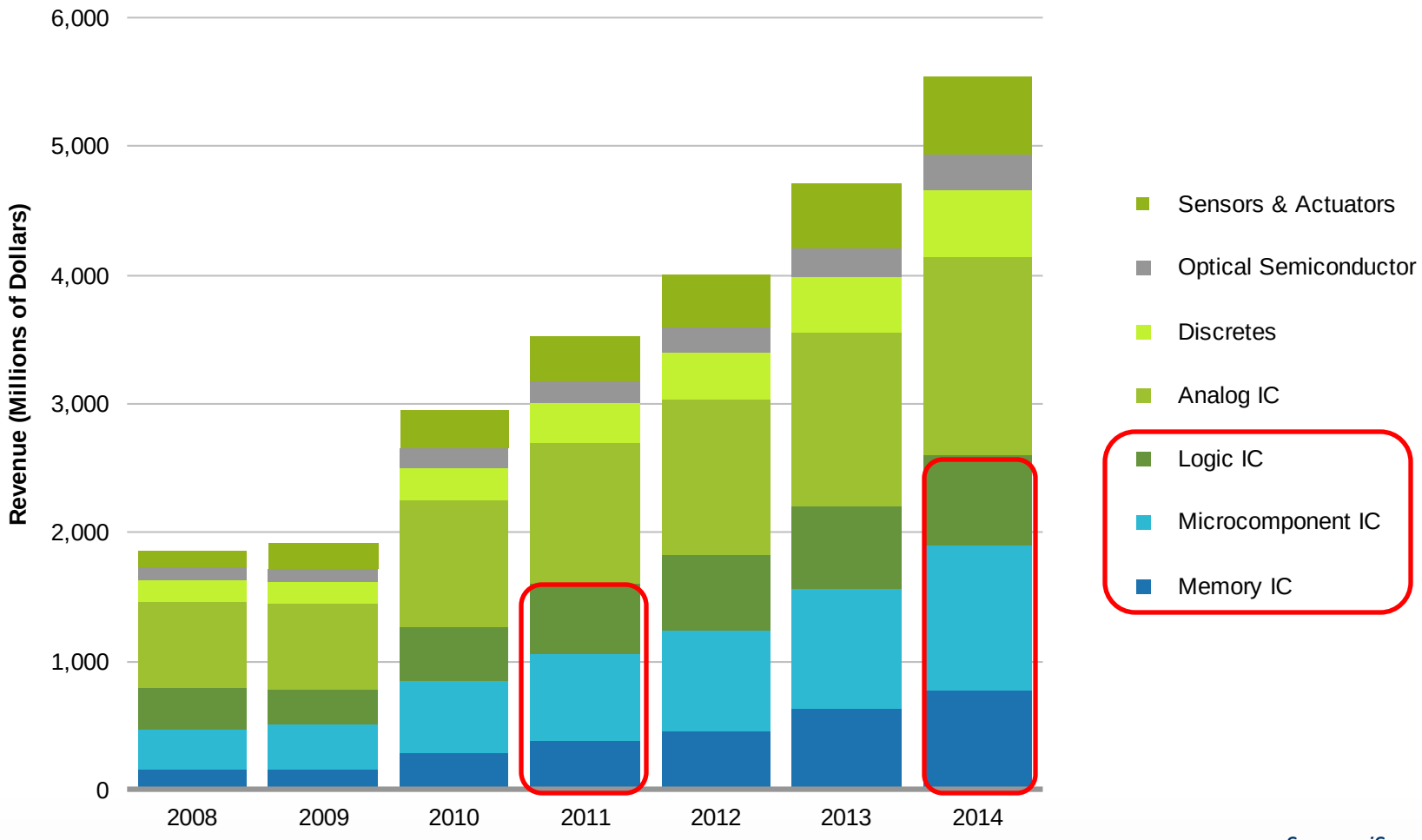
Regional Vehicle Production Trends

- China has become #1 of automobile vehicle production country since 2010
- The WW market share is 23.5% in 2010
- Automotive vehicle number up to 290 million in Sep. '11 in China



Source: iSuppli

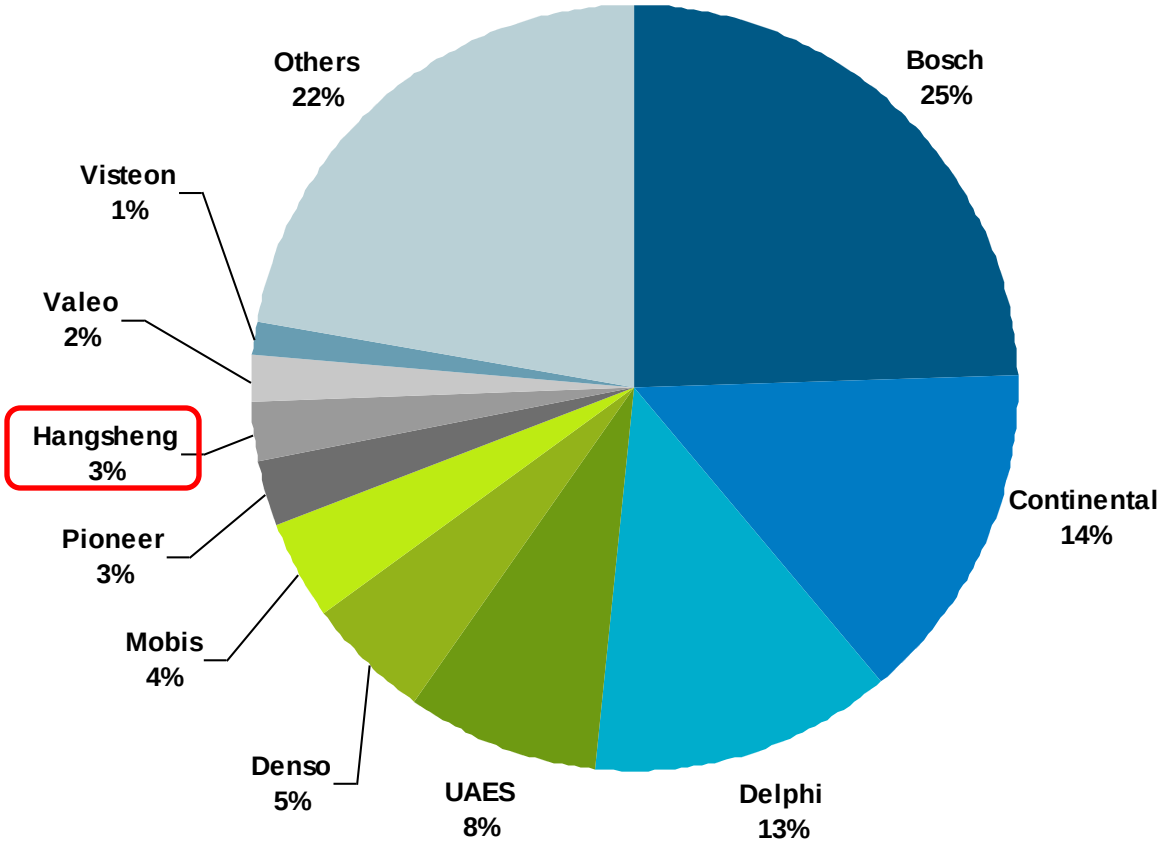
China Automotive Electronics Semiconductor Devices Consumption



Source: iSuppli

Leading Automotive Electronics Suppliers in China

- Limited market share from domestic brand suppliers

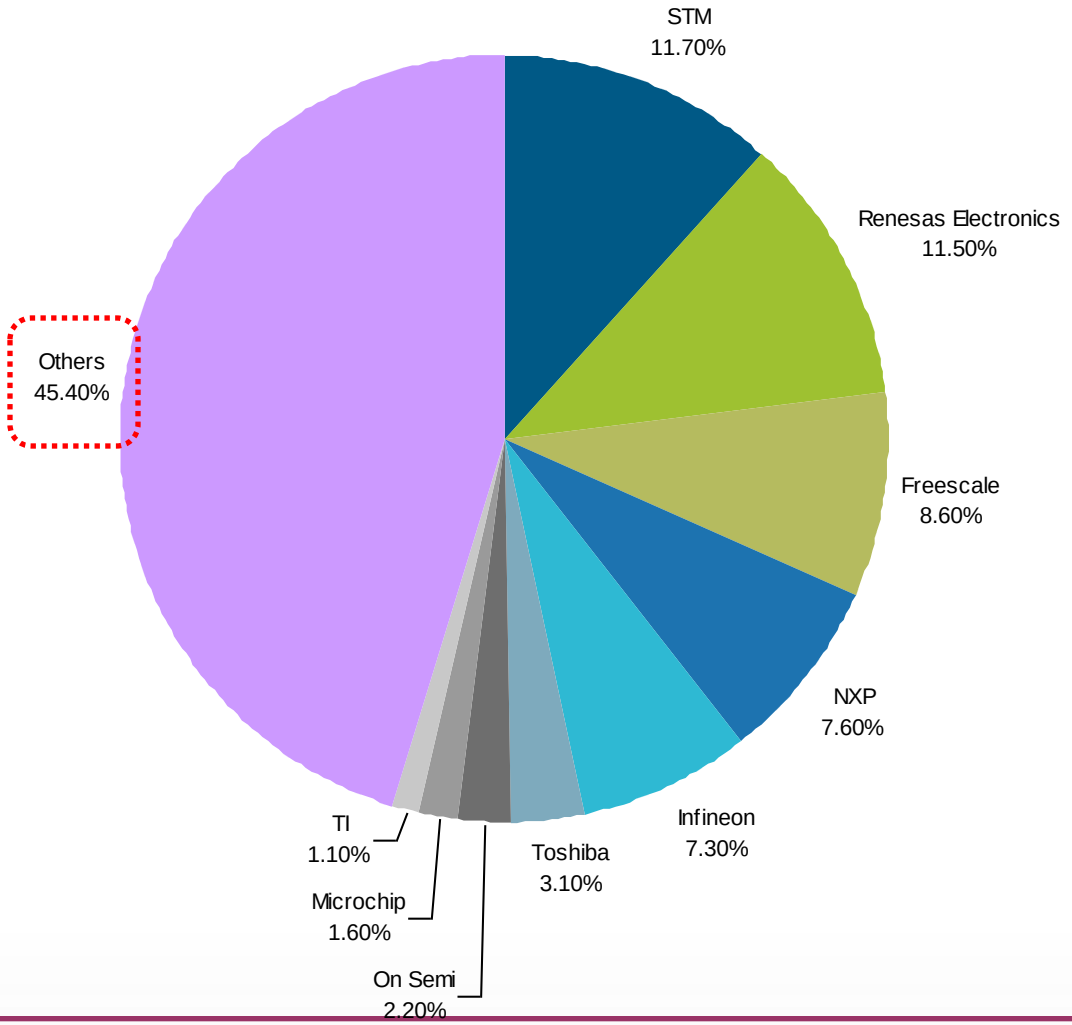


Leading automotive electronics suppliers in China, 2010

Source: iSuppli

Leading Automotive Electronics Semiconductor Vendors in China, 2010

- Again, few domestic brand companies even in semiconductor vendor list



Source: iSuppli

MCU in Automotive Applications

- eFlash-based MCU addresses wide applications (>100 units per advanced car)

Bits and Bytes for Different Vehicle Applications

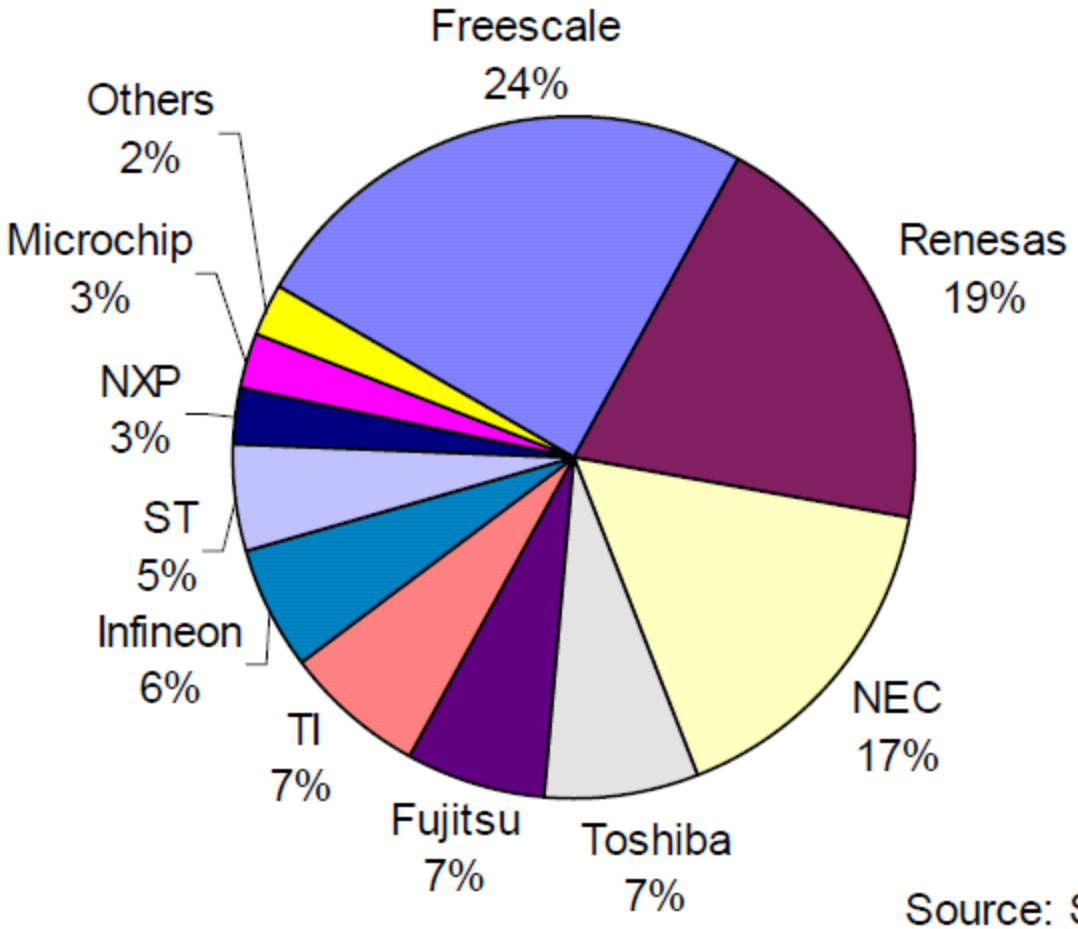
Computing Unit						
8-bit MCU	16-bit MCU	32-bit MCU	64-bit MPU	16-bit DSC	32-bit DSC	32-bit DSP
Maximum Memory						
1KB to 128KB	8KB to 1.5MB	256KB to 3MB	External	12KB to 512KB	256KB	
Applications						
Passive keyless entry	Hands-free telematics module	Active high-end electronic stability control	Voice recognition	Brushless DC motor control	Hybrid motor control	Vision-based driver assistance
TPMS	Airbags	Airbags	Video compression	Fuel pump	EPS	High-end audio systems
Body lighting	HVAC	Telematics	Navigation		Radar processing	
Rain sensor wiper control	Sunroof	Powertrain	Driver info system			
Power mirrors	Lane detection	Lane departure				
Reverse parking assist	Body electronics					
Smart sensors						
Network						
LIN/CAN	Low-/High-speed CAN	High-speed CAN, FlexRay, MOST	High-speed CAN, FlexRay, MOST	CAN	CAN	High-speed CAN, FlexRay, MOST

Source: Wards Auto

Source: IC Insights, 2011

Leading Automotive Electronics MCU Vendors in China

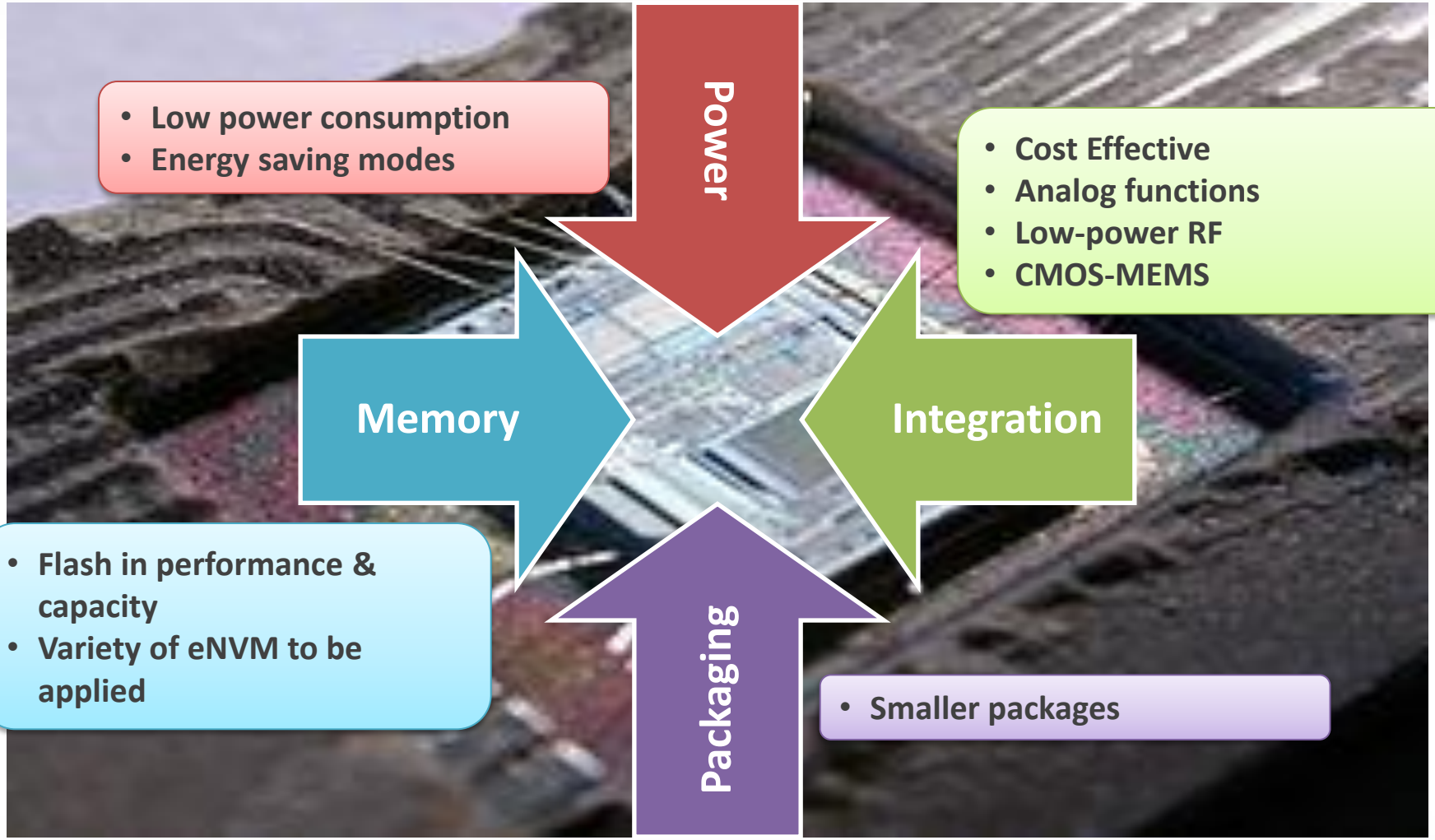
- NO domestic brand companies in MCU vendor list



Source: Strategy Analytics , 2008

Outline

IC Technology Trends



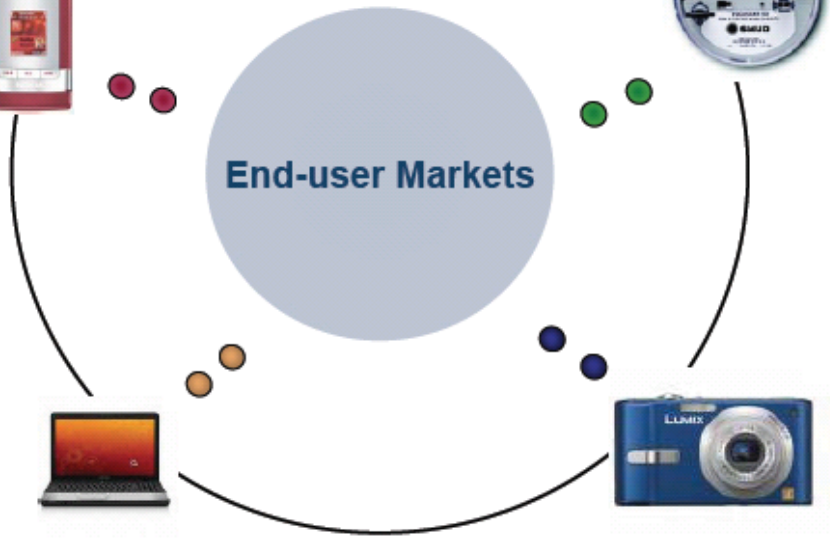
Key MCU End-User Market

✓ **GRACE Semiconductor Serves ALL !**

Automotive
Hybrid engine control unit (ECU), electronic power steering, tire pressure monitoring, electronic stability control, networking/multiplexing, and safety systems

Communications
Smart cards and cell phones

Industrial
Smart metering, LED lighting, advanced motor control, solar panels, and wind turbines



Computing
Digital power supplies, PC and peripherals

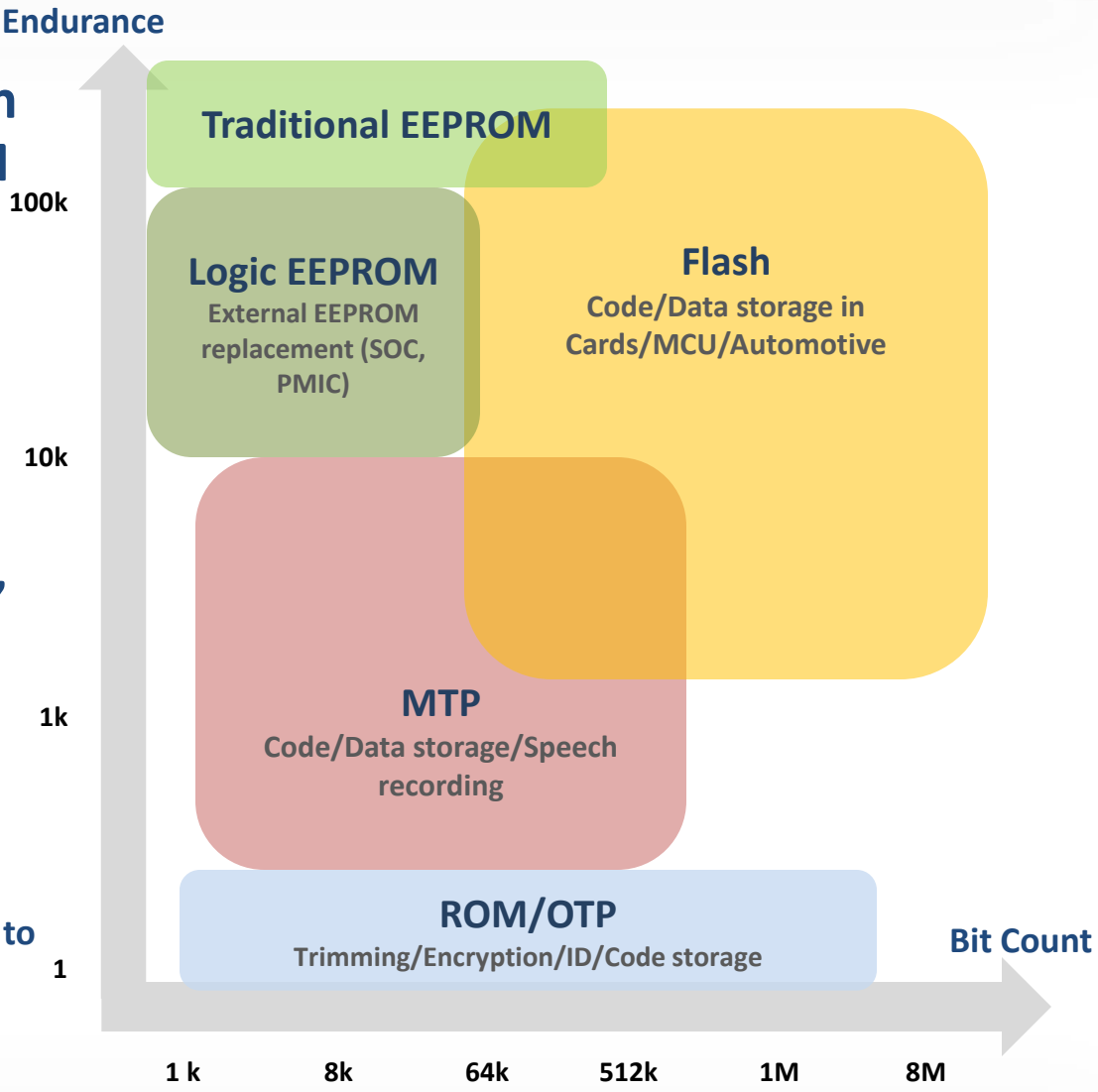
Consumer
Media players, digital cameras, white goods, and home security systems

NVM Technologies

- **Primary considerations on choosing embedded NVM**
  - Memory density, area;
  - P/E times, reliability;
  - Cost (extra masks);
  - Power consumption;

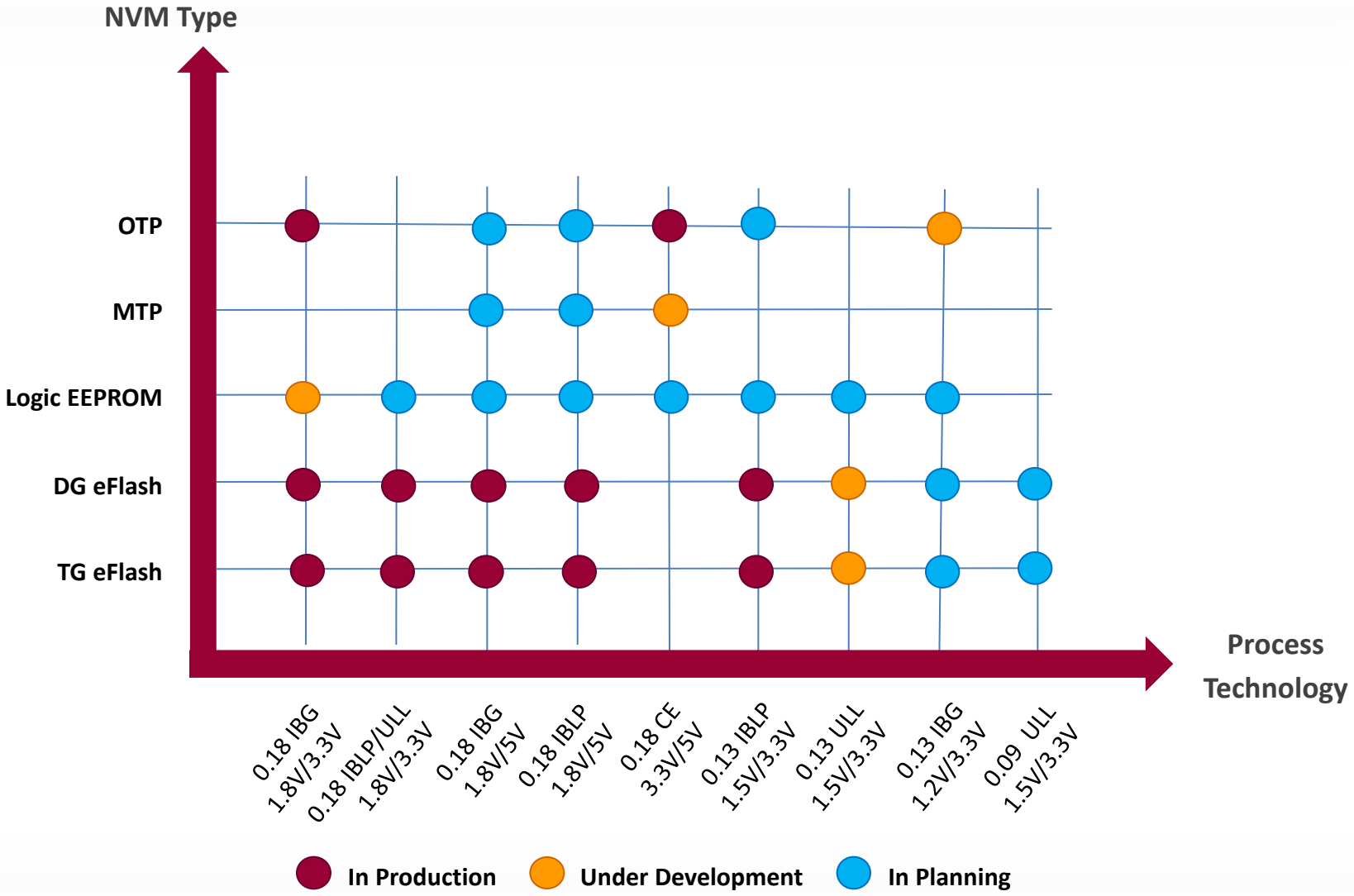
- **Flexible selections of OTP, EEPROM, MTP and Flash enables best trade-off by product-demand and manufacturing cost.**

Note: Logic EEPROM means fully compatible to logic process zero mask added.

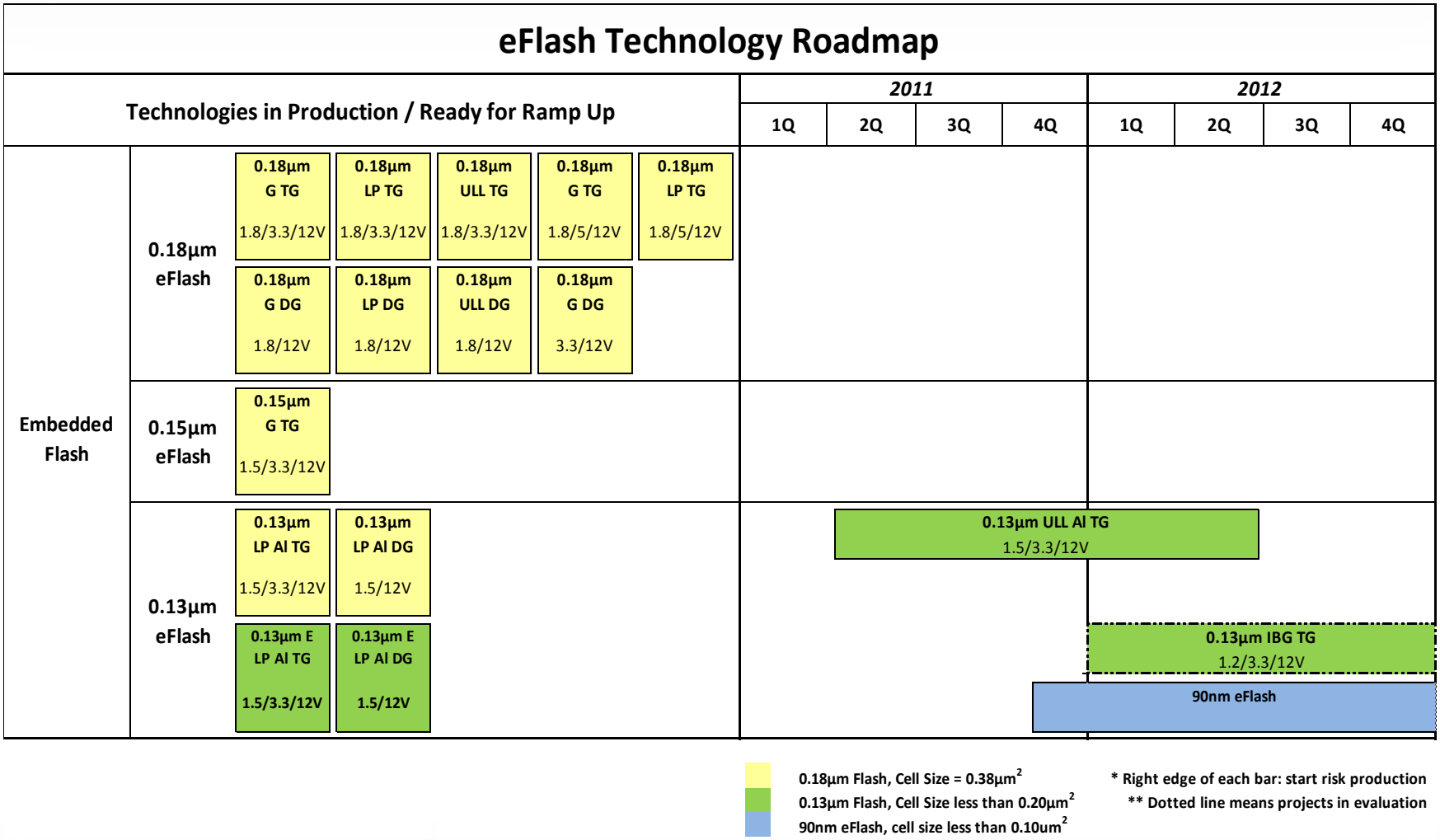


Outline

Extensive eNVM Platforms

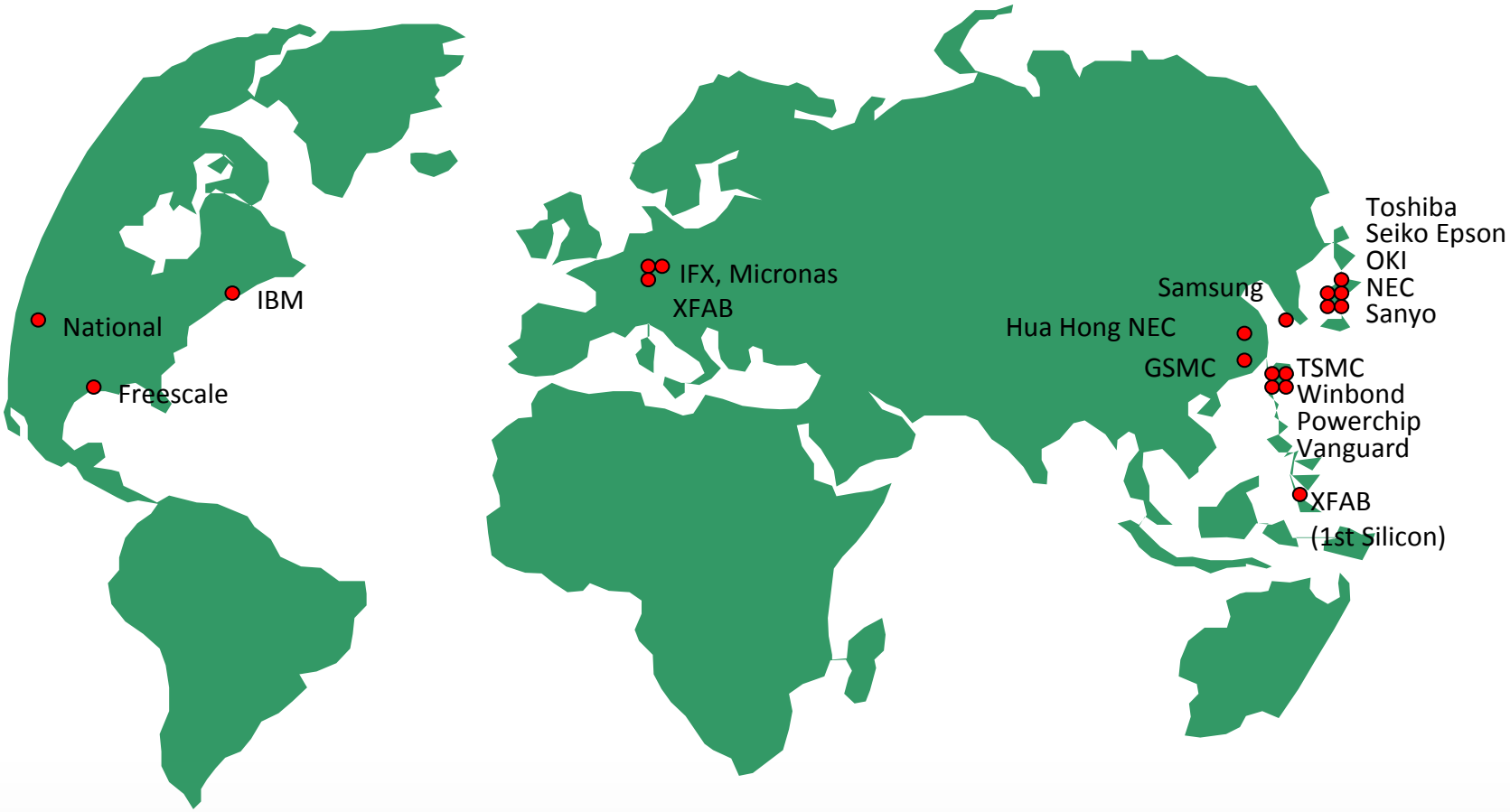


Platform eFlash Technology Roadmap



Why GRACE eFlash Technology

- Most robust and reliable Flash technology – SST " Self-Aligned " SuperFlash for advanced MCU and smart card applications.

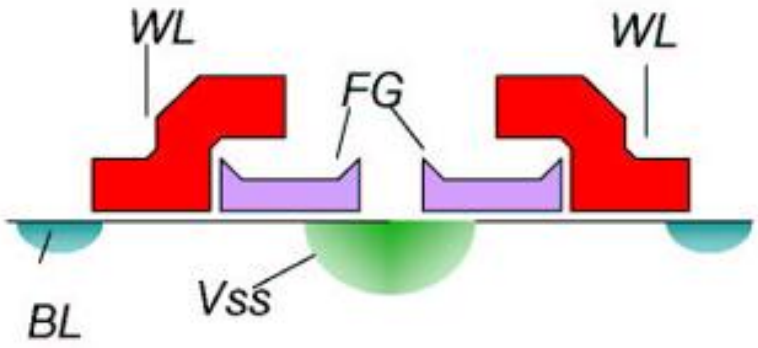


Why GRACE eFlash Technology

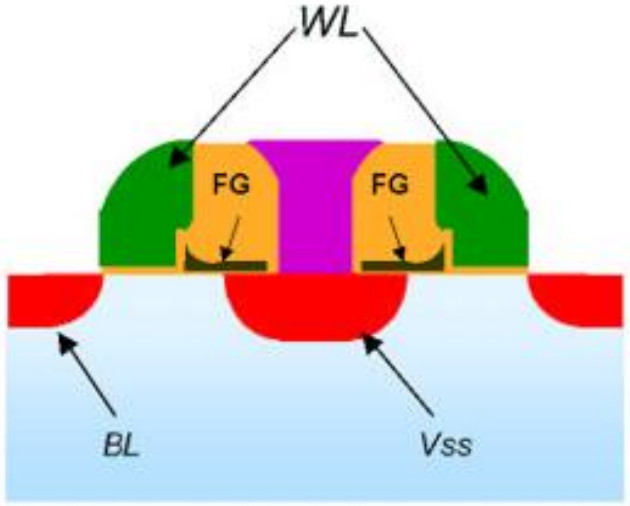
- **Most robust and reliable Flash technology – SST " Self-Aligned " SuperFlash for advanced MCU and smart card applications.**

- **Small cell size 0.38um² (0.18um) -> 0.197um² (0.13um) -> 0.1um²(90nm)**
  One generation smaller than non-self-align eFlash technology

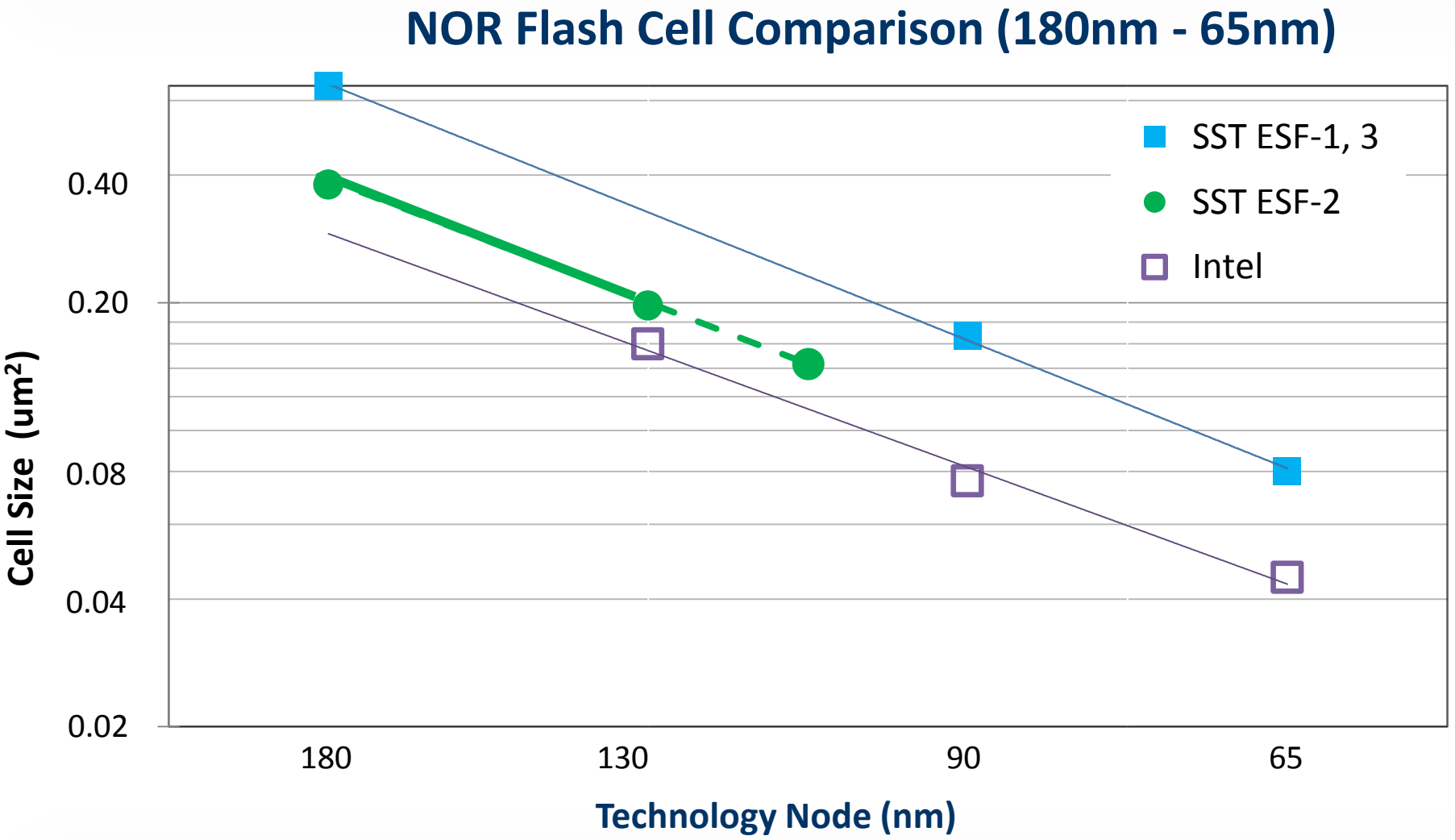
Conventional non-self-aligned cell



Self-aligned split gate cell

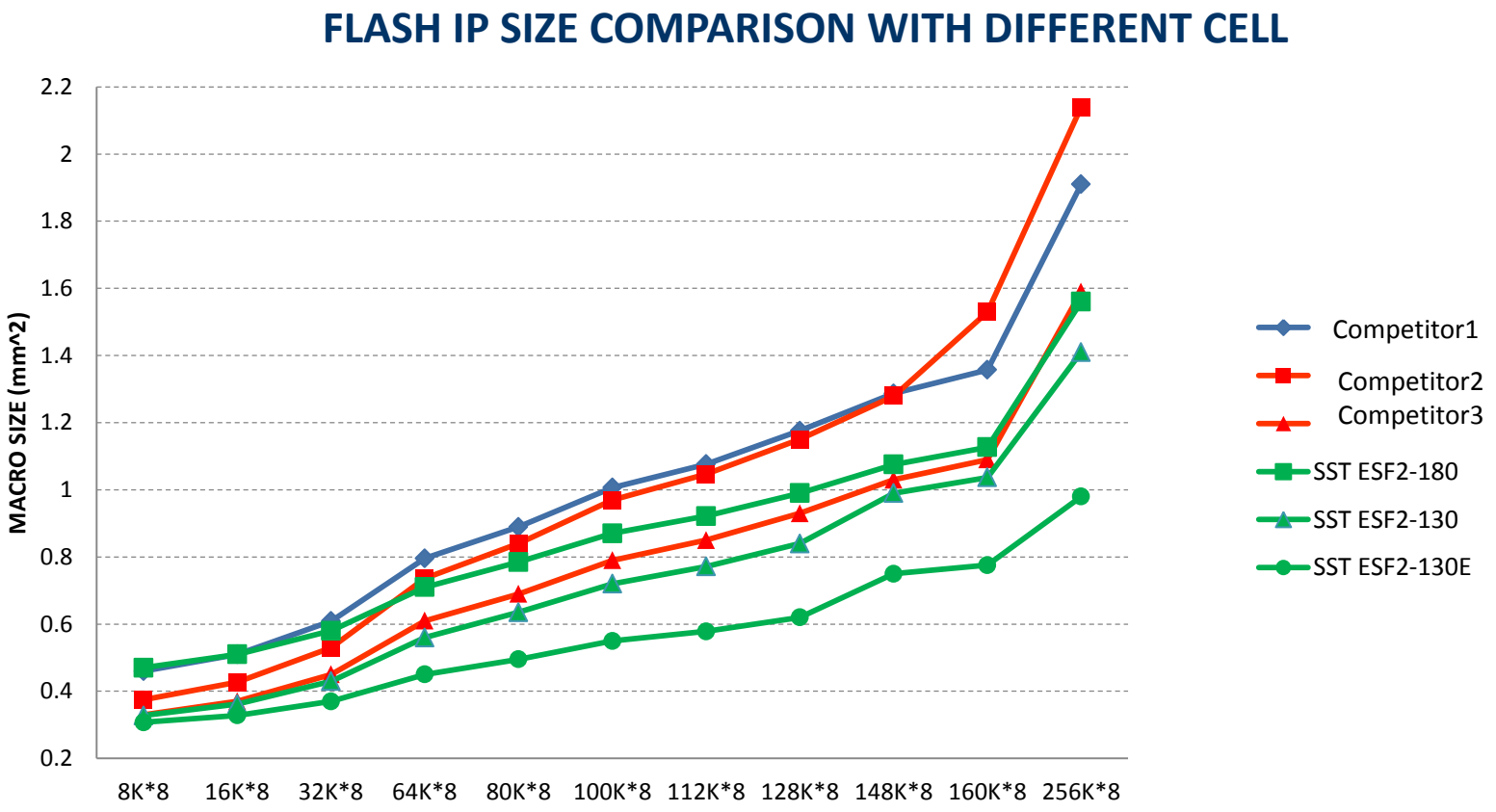


NOR Flash Cell Dimension Trend



GRACE Competitive Flash IP

- GRACE offers smaller Flash IP size.



SPICE Model Verification of 0.18µm Technology over Extended Temperature Range

- **Active Devices on 0.18µm LP Logic & eFlash technologies**
  - Models of 1.8V IBLP NMOS and PMOS verified over -40~**175**℃ for both 0.18µm IBLP logic process and 0.18µm IBLP eFlash process.
  - Models of 3.3V IBLP NMOS and PMOS verified over -40~**175**℃ for both 0.18µm IBLP logic process and 0.18um IBLP eFlash process.
  - Models of 5V NMOS and PMOS verified over -40~**175**℃ for 0.18µm IBLP logic process and 0.18µm IBLP eFlash process.

- **Passive Devices on 0.18µm Technology**
  - Model of MiM capacitor (irrespective of 0.18µm, IBG & IBLP) can support temperature up to **175**℃.
  - Model of HR Resistor (irrespective of 0.18µm, IBG & IBLP) can support temperature up to **175**℃.

GRACE eFlash Technology Summary

- 0.25/0.18/0.12um standalone NOR Flash in volume production since 2004, shipped around 700,000 wafers and continues
- 0.25um e-Flash engine controller in production since May/05
  - 0 PPM in 14 millions chips shipped (with ECC)
- 0.18um e-Flash in volume production since Jan/07, shipped over 100,000 wafers in last 24 months, and achieved 50+ product tape-out's so far
- 0.13um IBLP e-Flash in volume production since Jan/10
- Strong in-house design service and testing team for custom Flash IP design and testing
- Superior Flash IP reliability of endurance > 100K (with capability to 1000K) and 100 years data retention
- Low mask count eFlash technologies are available (26ML for 4 metal layers)

Outline

Automotive Quality Summary

- **Achieved ISO/TS16949 certification since 2005**
  - ✓ Quality management system compliant for automotive production
- **Certified for**
  - ✓ ISO14001 (Environmental)
  - ✓ OHSAS18001 (Safety and Health)
  - ✓ ISO27001 (Information Security)
  - ✓ Corporate Social Responsibility
  - ✓ Sony green manufacturing partner
- **Automotive success story**
  - ✓ Existing 4 automotive customers, several automotive products in mass production
  - ✓ Zero automotive products customer complaint in 2010
  - ✓ Established Zero Defect program for continuous improvement
  - ✓ Passed numerous Japan and US customers' automotive quality system audit
  - ✓ VDA6.3 Third Party Audit - Overall Degree of Conformity : 90.5%, Grade A @end/2010

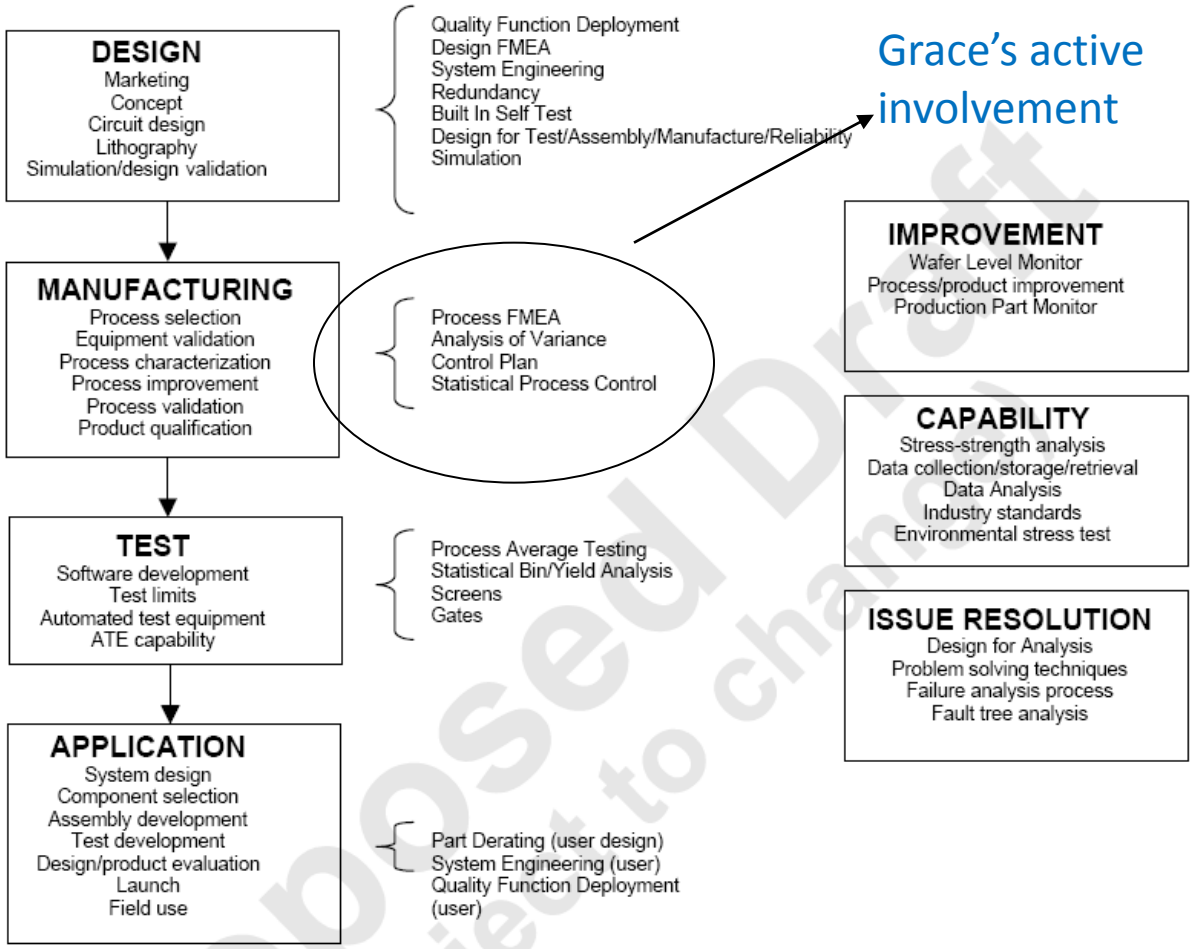
Grace System Certificate

Certified

- Quality System: ISO9001/TS16949
- Environment System: ISO14001
- Occupational Health and Safety System: OHSAS18001
- Information Security System: ISO27001 (BS7799)
- Corporate Social Responsibility: Certified by Shanghai Municipal Government

Definition of Zero Defect

AEC-Q004 Zero Defect Tools



Zero defects is defined as a part with no field failures, the combination of high-quality manufacturability and high-efficiency testability that has prevented any supplier-initiated defects from reaching end customer

Automotive Service Package Installed for Zero Defect Program

- **Additional methodology during wafer processing to achieve the goal of zero defect by variation reduction, early detection of abnormalities and screening of mavericks .**
- **Established automotive zero defect program for continual improvement**
  - ✓ Processing wafers on preferred tools
  - ✓ Additional defect inspection and tight limits
  - ✓ Additional Statistical Process Control rules and tight process capability targets
  - ✓ Additional wafer Acceptance Test control rules and tight acceptance criteria
  - ✓ Additional out-going inspection sites and tight acceptance criteria
  - ✓ Additional maverick parameters out of control handling
  - ✓ Process reliability limits characterization
  - ✓ Reduced rework strategy, do it right the first time
  - ✓ Statistical test screen at wafer sort, remove outliers from baseline distribution
  - ✓ Safe Launch (additional inspection) for new product ramp

Reference GSMC SOP# 005-500-019, Zero Defect Implementation Guideline

Requirements for Automotive IC

- **Automotive temperature grade**
  - Grade 0: 150℃ ambient
  - Grade 1: 125℃ ambient
  - Grade 2: 105℃ ambient
  - Grade 3: 85℃ ambient

Parameter	Consumer	Industrial	Automotive
Temperature	0°C - +40°C	-10°C - +70°C	-40°C - +155°C
Operation time	1-3 years	5-10 years	up to 15 years
Humidity	low	environment	0% - 100%
Tolerated field failure rates	<3%	<<1%	target: zero failures
Supply	up to 2 years	up to 5 years	up to 30 years

Source: Robert Bosch GmbH

Temperature	Driver interior	-40°C to +85°C
	Under hood	-40°C to +125°C
	On engine	-40°C to +150°C
	In the exhaust and combustion	-40°C to +200-600°C
Mechanical shock	During assembly (drop test)	3,000g
	On the vehicle	50-5,000g
Mechanical vibration		15g, 100Hz to 2KHz
Electromagnetic impulses		100 to 200V/m
Exposure	Common	Humidity, salt spray
	In some applications	Fuel, oil, brake fluid, transmission fluid, ethylene glycol, exhaust gases

Source: Toyota Motor Corp.

Automotive IC Qual. standard (AEC-Q100)

- High Temperature Operating Life
- Early Life Failure Rate
- Temperature Humidity Bias or HAST
- Autoclave or Unbiased HAST
- Temperature Cycle
- ESD Human Body Model or Machine Model
- ESD Charge Device Model
- Latch up

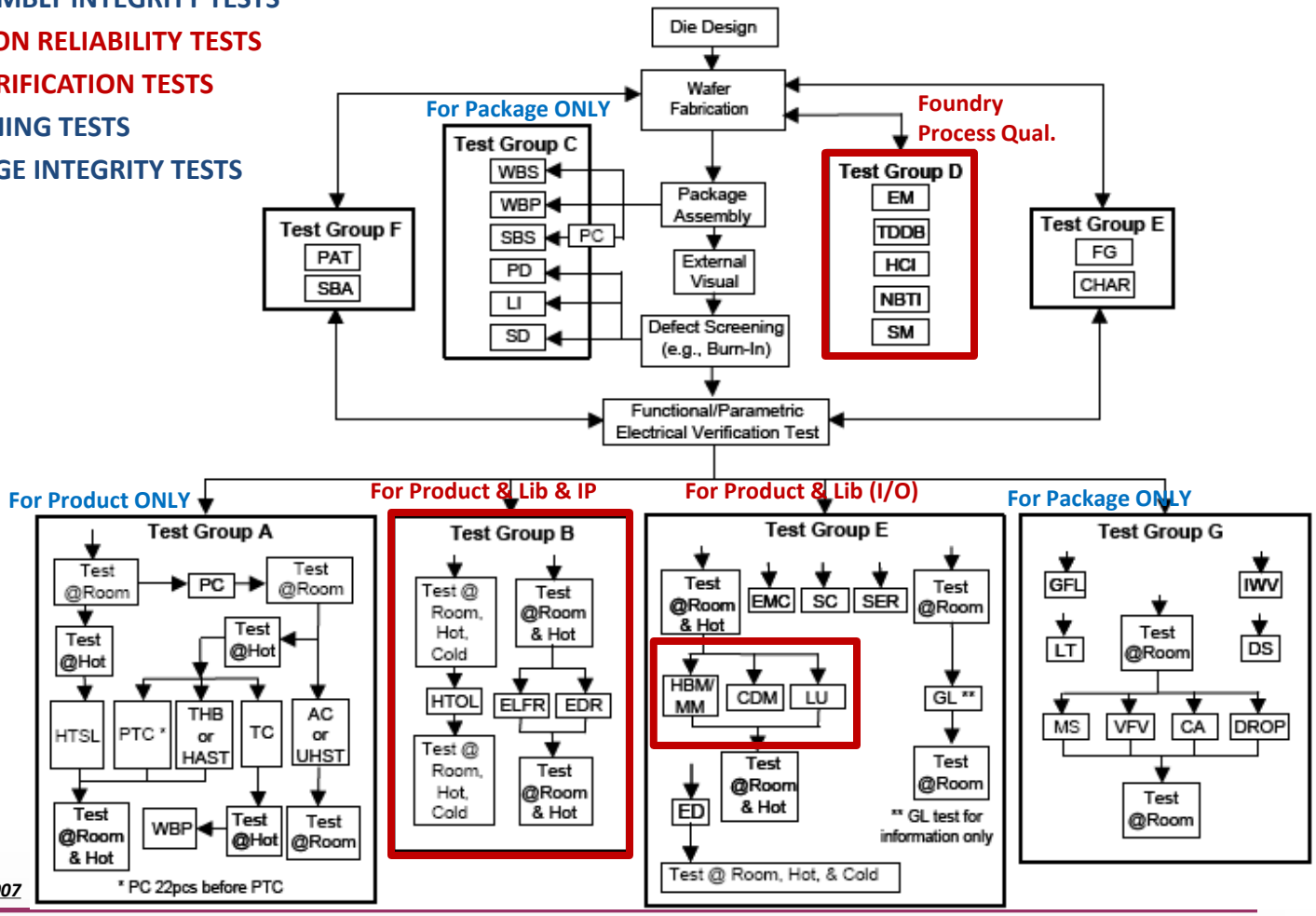
IC Product Qual

- ***NVM Endurance, Data Retention and Operational Life***
- ***Electromigration***
- ***Stress Migration***
- ***Time Dependent Dielectric Breakdown***
- ***Hot Carrier Injection***
- ***Negative Bias Temperature Instability***

IP and Process Qual

Qualification Flow for Process, Library&IP according to AEC-Q100

- TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS
- TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS
- TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS
- TEST GROUP D – DIE FABRICATION RELIABILITY TESTS
- TEST GROUP E – ELECTRICAL VERIFICATION TESTS
- TEST GROUP F – DEFECT SCREENING TESTS
- TEST GROUP G – CAVITY PACKAGE INTEGRITY TESTS



Note: IP here doesn't include library which contains I/Os.

Source: AEC - Q100 - Rev-G, May 14, 2007

AEC-Q100 Process Qualification Test Items

- **No specific lifetime requirement defined for process qual by AEC-Q100, data should be made available to user upon request.**

TEST GROUP D – DIE FABRICATION RELIABILITY TESTS								
STRESS	ABV	#	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS
Electromigration	EM	D1	---	---	---	---	---	The data, test method, calculations and internal criteria should be available to the user upon request for new technologies.
Time Dependent Dielectric Breakdown	TDDB	D2	---	---	---	---	---	The data, test method, calculations and internal criteria should be available to the user upon request for new technologies.

TEST GROUP D – DIE FABRICATION RELIABILITY TESTS (CONTINUED)								
STRESS	ABV	#	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS
Hot Carrier Injection	HCI	D3	---	---	---	---	---	The data, test method, calculations and internal criteria should be available to the user upon request for new technologies.
Negative Bias Temperature Instability	NBTI	D4	---	---	---	---	---	The data, test method, calculations and internal criteria should be available to the user upon request for new technologies.
Stress Migration	SM	D5	---	---	---	---	---	The data, test method, calculations and internal criteria should be available to the user upon request for new technologies.

Source: AEC - Q100 - Rev-G, May 14, 2007

Group B Test Items and Specifications – Applied to Library Test Chip

- **Group B**
  - HTOL
  - ELFR (optional)
  - EDR (NVM ONLY)

TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS								
STRESS	ABV	#	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS
High Temperature Operating Life	HTOL	B1	H, P, B, D, G, K	77	3	0 FAILS	JEDEC JESD22-A108	For devices containing NVM, endurance preconditioning must be performed before HTOL per Q100-005. **Grade 0:** +175°C T_a for 408 hours or +150°C T_a for 1000 hours. **Grade 1:** +150°C T_a for 408 hours or +125°C T_a for 1000 hours. **Grade 2:** +125°C T_a for 408 hours or +105°C T_a for 1000 hours. **Grade 3:** +105°C T_a for 408 hours or +85°C T_a for 1000 hours. **Grade 4:** +90°C T_a for 408 hours or +70°C T_a for 1000 hours. V_{cc} (max) at which dc and ac parametrics are guaranteed. Thermal shut-down shall not occur during this test. **TEST before and after HTOL at room, hot, and cold temperature.**
Early Life Failure Rate	ELFR	B2	H, P, B, N, G	800	3	0 FAILS	AEC Q100-008	Devices that pass this stress can be used to populate other stress tests. Generic data is applicable. **TEST before and after ELFR at room and hot temperature.**
NVM Endurance, Data Retention, and Operational Life	EDR	B3	H, P, B, D, G, K	77	3	0 FAILS	AEC Q100-005	**TEST before and after EDR at room and hot temperature.**

Group B Test Items and Specifications – Applied to IP Test Chip

- **Group B**
  - HTOL
  - EDR (NVM only)

TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS								
STRESS	ABV	#	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS
High Temperature Operating Life	HTOL	B1	H, P, B, D, G, K	77	3	0 FAILS	JEDEC JESD22-A108	For devices containing NVM, endurance preconditioning must be performed before HTOL per Q100-005. **Grade 0:** +175°C T_a for 408 hours or +150°C T_a for 1000 hours. **Grade 1:** +150°C T_a for 408 hours or +125°C T_a for 1000 hours. **Grade 2:** +125°C T_a for 408 hours or +105°C T_a for 1000 hours. **Grade 3:** +105°C T_a for 408 hours or +85°C T_a for 1000 hours. **Grade 4:** +90°C T_a for 408 hours or +70°C T_a for 1000 hours. V_{cc} (max) at which dc and ac parametrics are guaranteed. Thermal shut-down shall not occur during this test. **TEST before and after HTOL at room, hot, and cold temperature.**
Early Life Failure Rate	ELFR	B2	H, P, B, N, G	800	3	0 FAILS	AEC Q100-008	Devices that pass this stress can be used to populate other stress tests. Generic data is applicable. **TEST before and after ELFR at room and hot temperature.**
NVM Endurance, Data Retention, and Operational Life	EDR	B3	H, P, B, D, G, K	77	3	0 FAILS	AEC Q100-005	**TEST before and after EDR at room and hot temperature.**

Note: IP here doesn't include library which contains I/Os.

Group E Test Items and Specifications – Applied to Library Test Chip

- Group E
  - HBM/MM
  - CDM
  - LU

TEST GROUP E – ELECTRICAL VERIFICATION TESTS								
STRESS	ABV	#	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS
Pre- and Post-Stress Function/Parameter	TEST	E1	H, P, B, N, G	All	All	0 Fails	Test program to supplier data sheet or user specification	Test is performed as specified in the applicable stress reference and the additional requirements in Table 2 and illustrated in Figure 2. Test software used shall meet the requirements of Q100-007. All electrical testing before and after the qualification stresses are performed to the limits of the individual device specification in temperature and limit value.
Electrostatic Discharge Human Body Model / Machine Model	HBM / MM	E2	H, P, B, D	See Test Method	1	0 Fails 2KV HBM (H2 or better) 200V MM (M3 or better)	AEC Q100-002 Q100-003	**TEST before and after ESD at room and hot temperature.** At least one of these models must be performed. Device shall be classified according to the maximum withstand voltage level. Device levels <2000V HBM and/or <200V MM require specific user approval.
Electrostatic Discharge Charged Device Model	CDM	E3	H, P, B, D	See Test Method	1	0 Fails 750V corner pins, 500V all other pins (C3B or better)	AEC Q100-011	**TEST before and after ESD at room and hot temperature.** Device shall be classified according to the maximum withstand voltage level. Device levels <750V corner pins and/or <500V all other pins CDM require specific user approval.

TEST GROUP E – ELECTRICAL VERIFICATION TESTS (CONTINUED)								
STRESS	ABV	#	NOTES	SAMPLE SIZE / LOT	NUMBER OF LOTS	ACCEPT CRITERIA	TEST METHOD	ADDITIONAL REQUIREMENTS
Latch-Up	LU	E4	H, P, B, D	6	1	0 Fails	AEC Q100-004	See attached procedure for details on how to perform the test. **TEST before and after LU at room and hot temperature.**

0.18µm eFlash Process
AEC Grade 1 Qualification Status

Technology	Voltage (V)	Qual Item					Status	Comment
		TDDB	HCI	NBTI	EM	SM		
0.18um eFlash IBG	1.8 / 3.3	P	P	P	P	P	√	
0.18um eFlash IBLP	1.8 / 3.3	P	P	P	P	P	√	
0.18um eFlash IBG	1.8 / 5	P[1]	P	P	P	P	√	accumulative HV Pcap gate oxide area < 0.46 mm^2
0.18um eFlash IBLP	1.8 / 5	P[1]	P	P	P	P	√	accumulative HV Pcap gate oxide area < 0.46 mm^2

- **0.18µm IBLP 1.8V/5V/12~60V scalable CDMOS – process fully qualification will be finished in 2012Q1**

0.18µm Flash IP
AEC Grade 1 Qualification Status

- **Test vehicle: 512K Bits Flash IP**

Test item		Test conditions	Sample size/Lot	#lot	Pass criteria	Lot No.	Result out date		
PLR	Endurance cycling	100K erase/write cycles at room temp. Electrical test pre-and post-stress at 25C and 125C	77	3	0 failure	Read	100K		
						1st	0/77		
						2nd	0/77		
						3rd	0/77		
	HTOL	150C for 408hrs, 1.21* Vdd, with checkboard and inverse checkboard pattern. 100K erase/write cycles at 25C.prior to it. Read at 96, and 408hrs.Electrical test pre-and post-stress at 25C, -40C and 125C	77	3	0 failure	Read	96hrs	408hrs	
						1st	0/77	0/77	
						2nd	0/77	0/77	
						3rd	0/77	0/77	
	Data retention	150C for 1008hrs,100K erase/write cycles at 25C. prior to it. Read at 168, 504 and 1008hrs Electrical test pre-and post-stress at 25C and 125C	77	3	0 failure	Read	168hrs	504hrs	1008hrs
						1st	0/77	0/77	0/77
						2nd	0/77	0/77	0/77
						3rd	0/77	0/77	0/77

0.13µm LP eFlash Process
AEC Grade 1 Qualification Status

Test Item	DUT failure definition	Spec	Device	Test result / year	Judgment
TDDB	First breakdown (hard or soft)	Lifetime under 1PPM cumulative failure rate > 3 year at 125℃,1.1*Vcc,10mm2. (Weibull distribution)	LV Ncap	12.8	Pass
			LV Pcap	3 (constrain max GOX area to 7.3 mm2)	Pass
			MV Ncap	623.6	Pass
			MV Pcap	14.9	Pass
			HV Ncap	10.7	Pass
			HV Pcap	3 (constrain max GOX area to 0.94 mm2)	Pass
HCI	Idsat shift > 10%	Lifetime under 1PPM cumulative failure rate > 0.06 year at 25℃,1.1*Vcc,DC. (Lognormal distribution)	LV NMOS	5.18	Pass
			LV PMOS	4.85E+04	Pass
			MV NMOS	0..2	Pass
			MV PMOS	10.49	Pass
			HV NMOS	3.36E+03	Pass
			HV PMOS	1.86E+04	Pass
NBTI	Idsat shift > 10%	Lifetime under 1PPM cumulative failure rate > 1.5 year at 125℃,1.1*Vcc,DC. (Lognormal distribution)	LV PMOS	4.75	Pass
			MV PMOS	10.13	Pass
EM	Resist increase > 10%	Lifetime under 1PPM cumulative failure rate > 3 year at 125℃,Jedr. (Lognormal distribution)	M1	3 (constrain max current density to 0.36 mA/µm)	Pass
			M2-6	3 (constrain max current density to 0.31 mA/µm)	Pass
			MT	9.46	Pass
			CT	3 (constrain max current density to 0.07 mA/CT)	Pass
			Via 1	5.32	Pass
			Via2-5	9.15	Pass
			Via stack	35.50	Pass
SM	Resist increase > 10%	Zero DUT fai after 1000 hours baking at 175℃,225℃,275℃	M1	No DUT fail	Pass
			M2-6	No DUT fail	Pass
			MT	No DUT fail	Pass

Outline

Strong Focus on Automotive Solutions

- **Grace Automotive Quality Executive Summary**
  - Zero defect program installed
  - Achieved ISO/TS16949 certification since 2005
  - Passed numerous Japanese and US customers/end customers quality system audits
    - Best quality award from a Japanese customer
    - Excellent score for US customer automotive audit
    - Achieved grade A of VDA 6.3 – German automotive quality standard

- **Substantial experience for automotive transfers with zero field return**
  - 0.25µm Embedded Flash – engine control and airbag control systems
  - 0.18µm Flash – radio and navigation systems
  - 0.35um SONOS Flash – infotainment system
  - 0.15um Logic – audio system

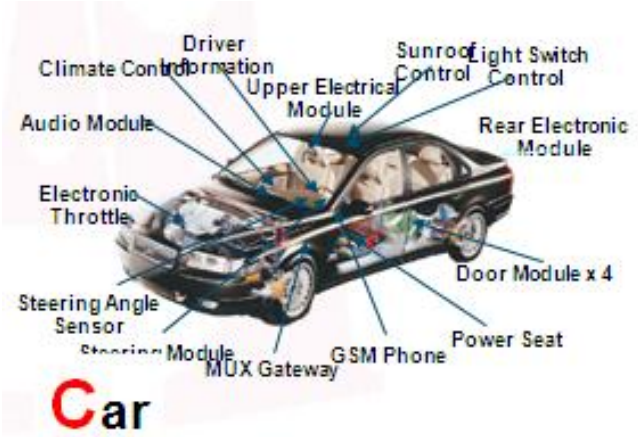
- **Complementary automotive offering via platform solutions**
  - 0.18µm SPICE models characterized to -40~175℃
  - 0.18µm embedded Flash process passed automotive process qualification
  - Flash IP Macro passed AEC-Q100 Grade 1 qualification

Grace Automotive Program Development

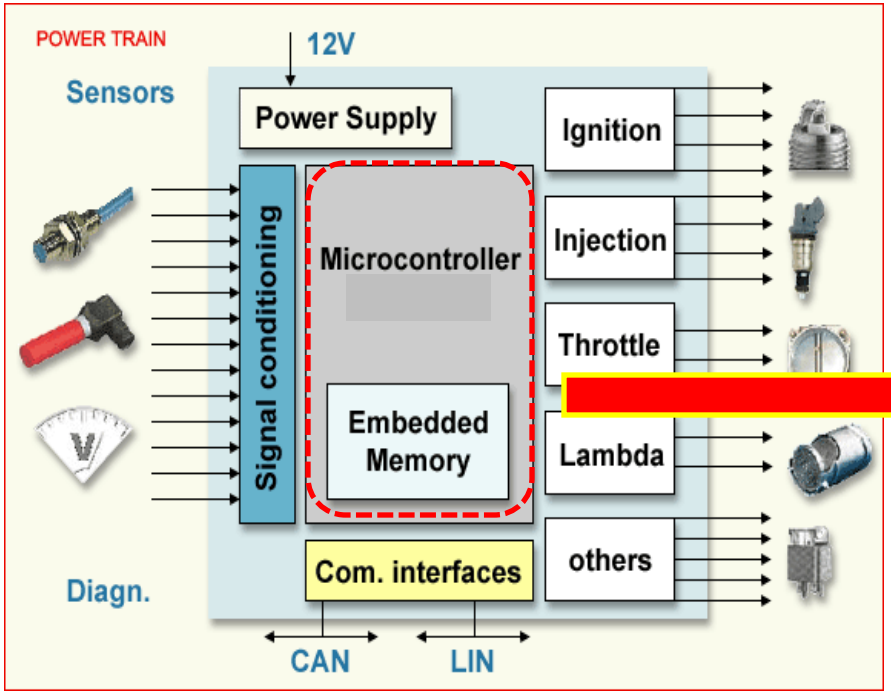
- **Complementary automotive offering via platform solutions**
  - 0.18µm Ultra Low Leakage technology & its library is under AEC-Q100 standard qualification
  - More Flash IP Macros are under AEC-Q100 Grade 1 (Ta=125C) qualification

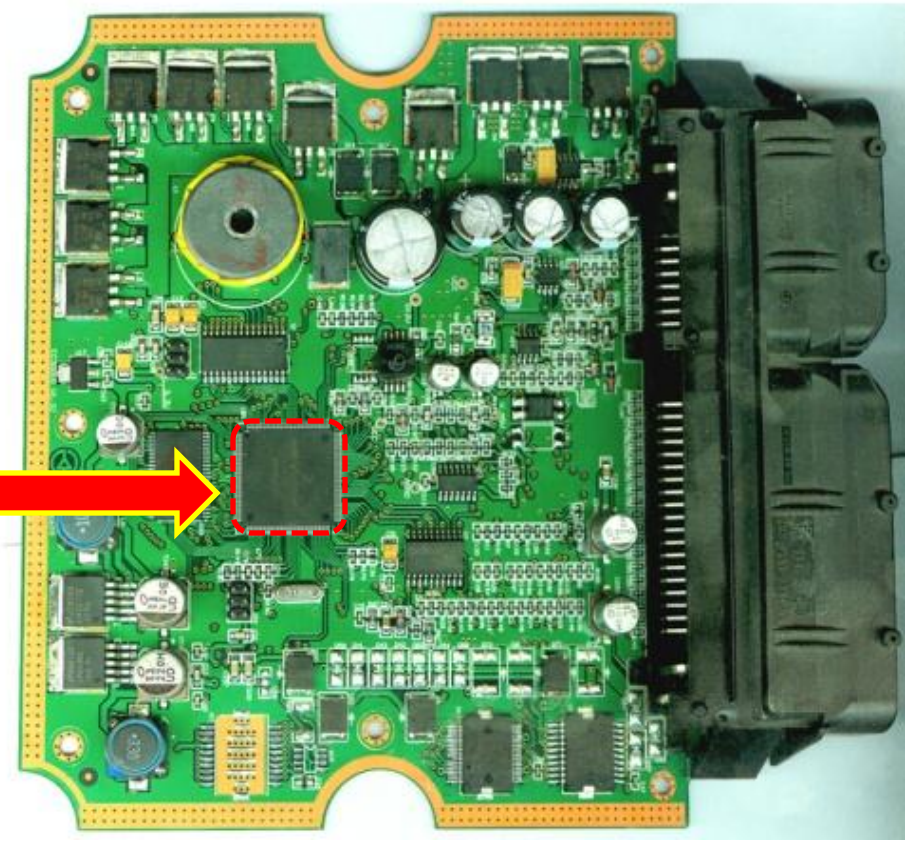
- **Alliance with industry, academy and research**

- **Industry alliance**
  - ECU (Electronic Control Unit) Module maker
    - Gasoline, Diesel , Hybrid engine
    - Infotainment , Central Stack, body control
    - Air-bag
  - IC design house
    - International brand companies
    - Domestic companies



Grace Automotive Program Development





Outline

Summary

- China provides a huge automotive market with strong OE companies;
- Fast Growing ECU makers are successful in infotainment and body control;
- Domestic Fab's are getting maturer;
- GRACE's world class E-Flash Technology can meet Automotive MCU requirements (Process, IP, and Quality control).;
- IC design is a weak point in the local supply chain so far;
- Industrial alliance is key for the incubation of this important industry;

Thank you!